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420 Chapter 4 The Processor 4121 [5] <45> What is the clock cycle time in a pipelined and non-pipelined processor? 4122 [10] <45> What is the total latency of an LWructioninst in a pipelined and non-pipelined processor? 4123 [10]f <45> I we can split ...

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Edition only, Exercise 18: Data table for Exercise 18 is incorrect Table should read: 2 182 In the second table on page 182 the code for table row (a) is incorrect slli instruction should be sll

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